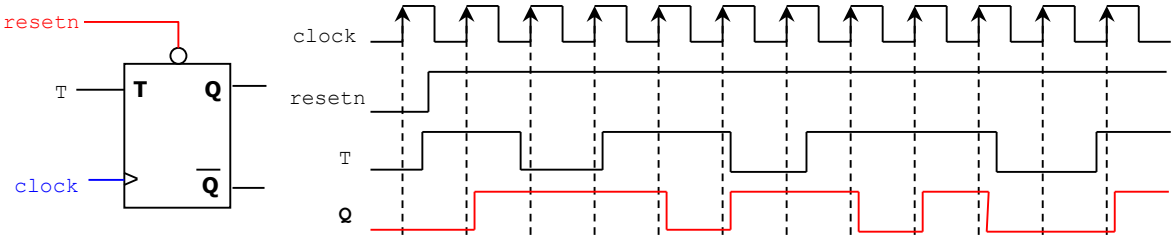
Solutions - Homework 3

(Due date: March 16th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

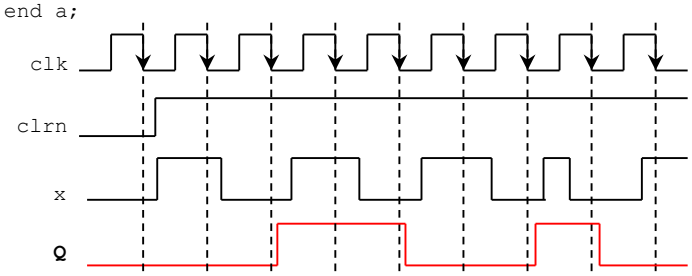
PROBLEM 1 (25 PTS)

a) Complete the timing diagram of the circuit shown below. (5 pts)

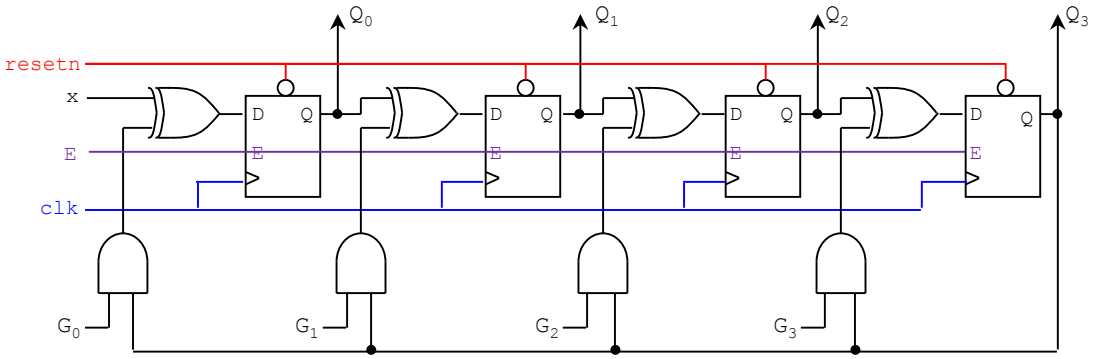


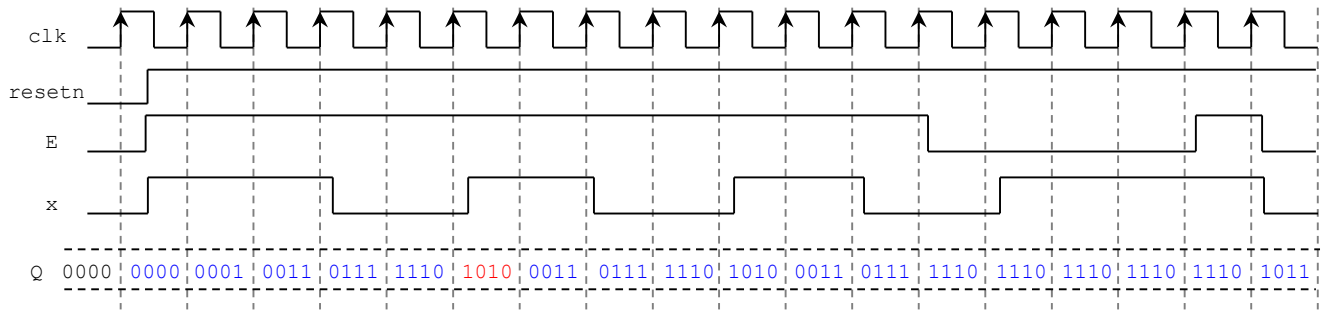
b) Complete the timing diagram of the circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( clrn, x, clk: in std_logic;
         q: out std_logic);
end circ;

architecture a of circ is

   signal qt: std_logic;

begin
   process (clrn, clk, x)
   begin
     if clrn = '0' then
        qt <= '0';
     elsif (clk'event and clk = '0') then
        if x = '0' then
           qt <= not(qt);
        end if;
     end if;
   end process;
   q <= qt;
end a;
```



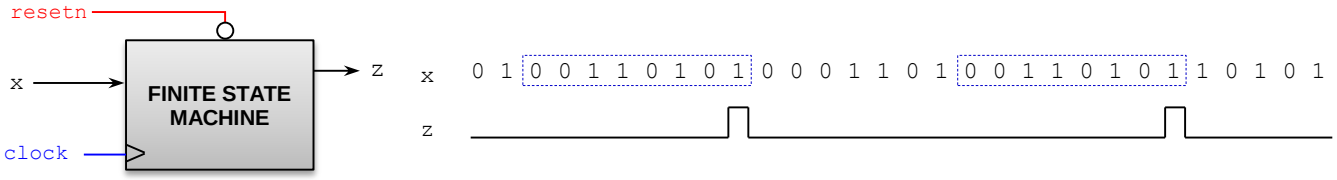
c) Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 0110$, $Q = Q_3Q_2Q_1Q_0$ (15 pts)



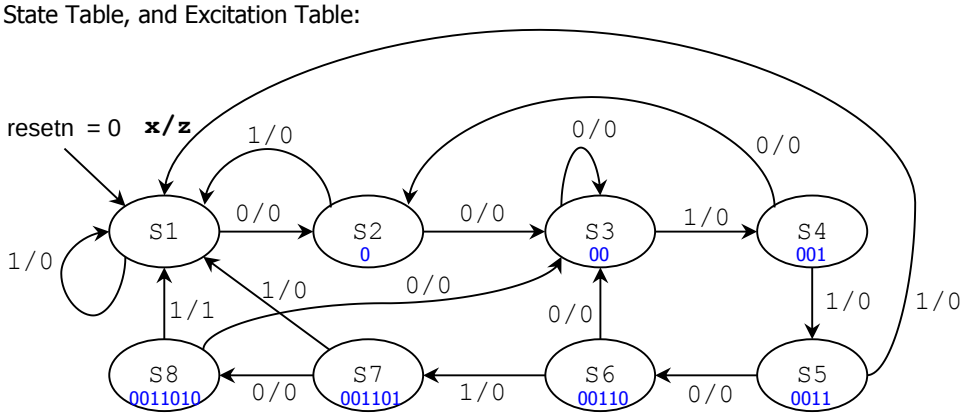


PROBLEM 2 (28 PTS)

- Sequence detector: The machine generates $z = 1$ when it detects the sequence 00110101. Once the sequence is detected, the circuit looks for a new sequence.
  - ✓ Draw the state diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. Is this a Mealy or a Moore Machine? Why? (17 pts)
  - ✓ Provide the excitation equations (simplify your circuit using K-maps). (6 pts)
  - ✓ Sketch the circuit. (5 pts)



- State Diagram, State Table, and Excitation Table:



x	PRESENT STATE	NEXT STATE	z
0	S1	S2	0
0	S2	S3	0
0	S3	S3	0
0	S4	S2	0
0	S5	S6	0
0	S6	S3	0
0	S7	S8	0
0	S8	S3	0
1	S1	S1	0
1	S2	S1	0
1	S3	S4	0
1	S4	S5	0
1	S5	S1	0
1	S6	S7	0
1	S7	S1	0
1	S8	S1	1

x	PRESENT STATE $Q_2Q_1Q_0$ (t)	NEXTSTATE $Q_2Q_1Q_0$ (t+1)	z
0	0 0 0	0 0 1	0
0	0 0 1	0 1 0	0
0	0 1 0	0 1 0	0
0	0 1 1	0 0 1	0
0	1 0 0	1 0 1	0
0	1 0 1	0 1 0	0
0	1 1 0	1 1 1	0
0	1 1 1	0 1 0	0
1	0 0 0	0 0 0	0
1	0 0 1	0 0 0	0
1	0 1 0	0 1 1	0
1	0 1 1	1 0 0	0
1	1 0 0	0 0 0	0
1	1 0 1	1 1 0	0
1	1 1 0	0 0 0	0
1	1 1 1	0 0 0	1

State Assignment:
S1: Q = 000 S2: Q = 001 S3: Q = 010 S4: Q = 011
S5: Q = 100 S6: Q = 101 S7: Q = 110 S8: Q = 111

This is a Mealy Machine. The output 'z' depends on the input as well as the present state.

- Minimization, Excitation equations, and circuit implementation:

$$Q_2(t+1) = \bar{x}Q_2\overline{Q_0} + xQ_2\overline{Q_1}Q_0 + x\overline{Q_2}Q_1Q_0 = \bar{x}Q_2\overline{Q_0} + xQ_0(Q_2 \oplus Q_1)$$
$$Q_1(t+1) = \overline{Q_2}Q_1\overline{Q_0} + \bar{x}Q_2Q_1 + \bar{x}\overline{Q_1}Q_0 + Q_2\overline{Q_1}Q_0 = \overline{Q_2}Q_1\overline{Q_0} + \bar{x}Q_2Q_1 + \overline{Q_1}Q_0(\bar{x} + Q_2)$$
$$Q_0(t+1) = \bar{x}\overline{Q_1}\,\overline{Q_0} + \bar{x}Q_2\overline{Q_0} + \bar{x}\overline{Q_2}Q_1Q_0 + x\overline{Q_2}Q_1\overline{Q_0} = \bar{x}\overline{Q_0}(\overline{Q_1} + Q_2) + \overline{Q_2}Q_1(x \oplus Q_0)$$
$$z = xQ_2Q_1Q_0$$

$Q_2(t+1)$

Q_1Q_0 \ xQ_2	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	0	0	0	1
10	0	1	0	0

$Q_1(t+1)$

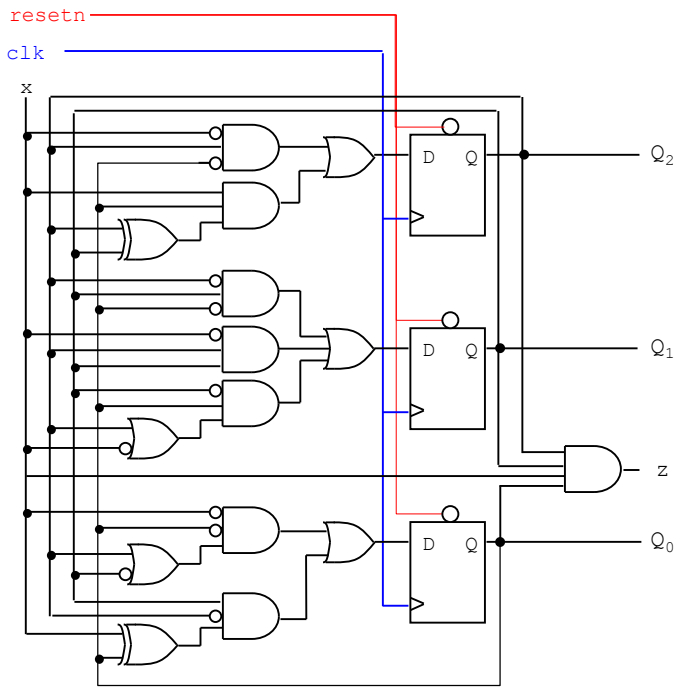
Q_1Q_0 \ xQ_2	00	01	11	10
00	0	0	0	0
01	1	1	1	0
11	0	1	0	0
10	1	1	0	1

$Q_0(t+1)$

Q_1Q_0 \ xQ_2	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	1	0	0	0
10	0	1	0	1

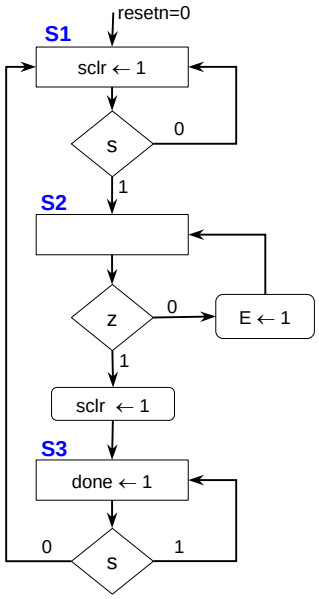
z

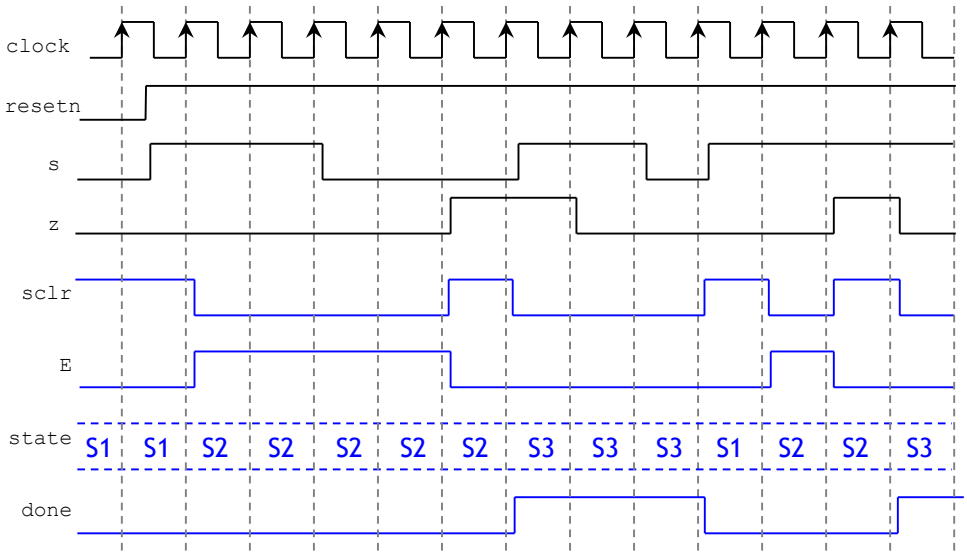
Q_1Q_0 \ xQ_2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	0
10	0	0	0	0



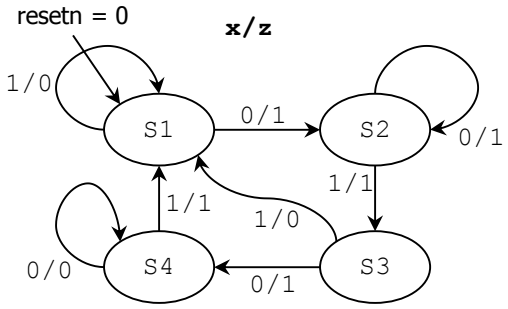
PROBLEM 3 (37 PTS)

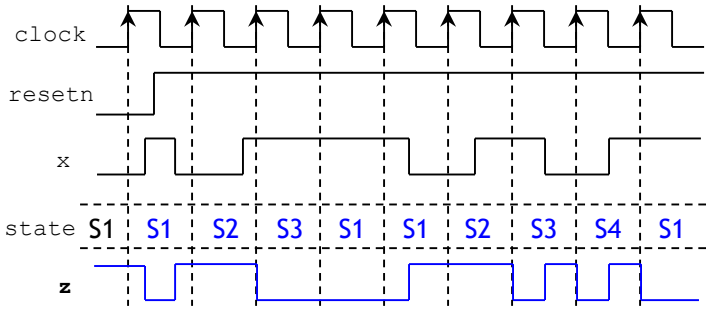
- Complete the timing diagram of the following FSM (represented as an ASM chart). (10 pts)



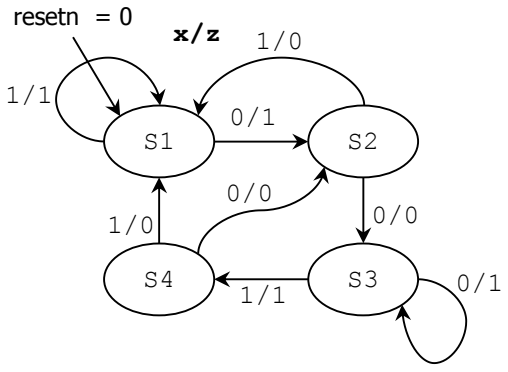


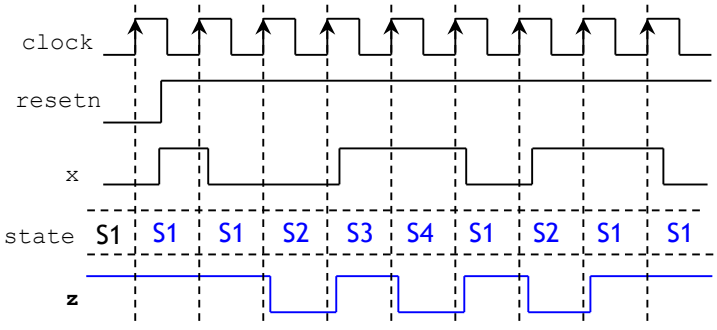
- Complete the timing diagram of the following FSMs. Are these Mealy or Moore machines? Why? (10 pts)





This is a Mealy Machine. The output 'z' depends on the input as well as the present state.

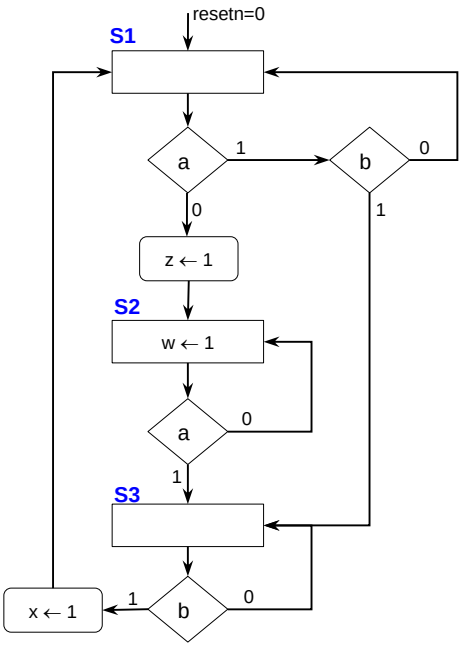




This is a Moore Machine. The output 'z' only depends on the present state.

- Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (17 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end myfsm;
```




```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
              if b = '1' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if a = '0' then y <= S2; else y <= S3; end if;

          when S3 =>
            if b = '1' then y <= S1; else y <= S3; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '0' then z <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if b = '1' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```